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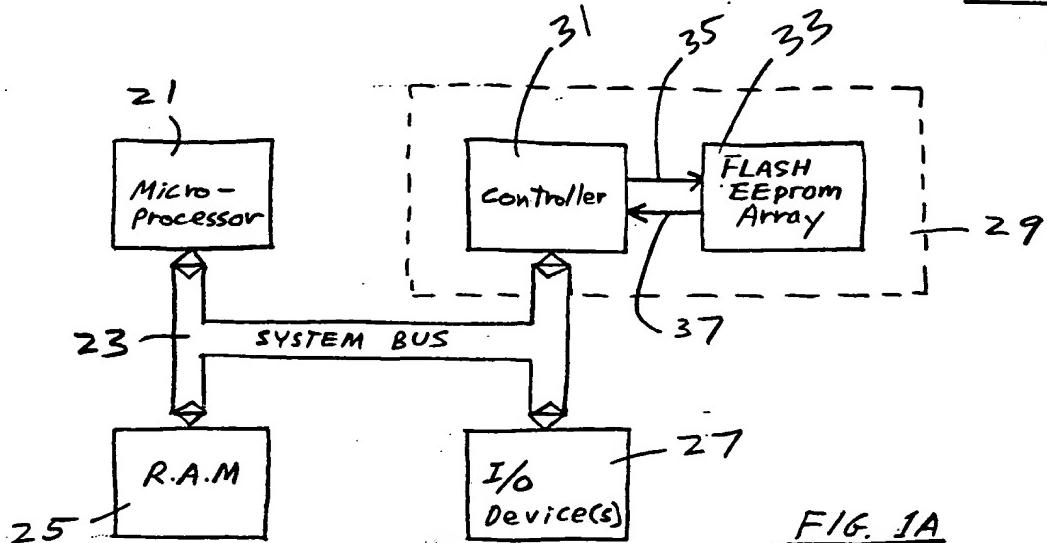


FIG. 1A

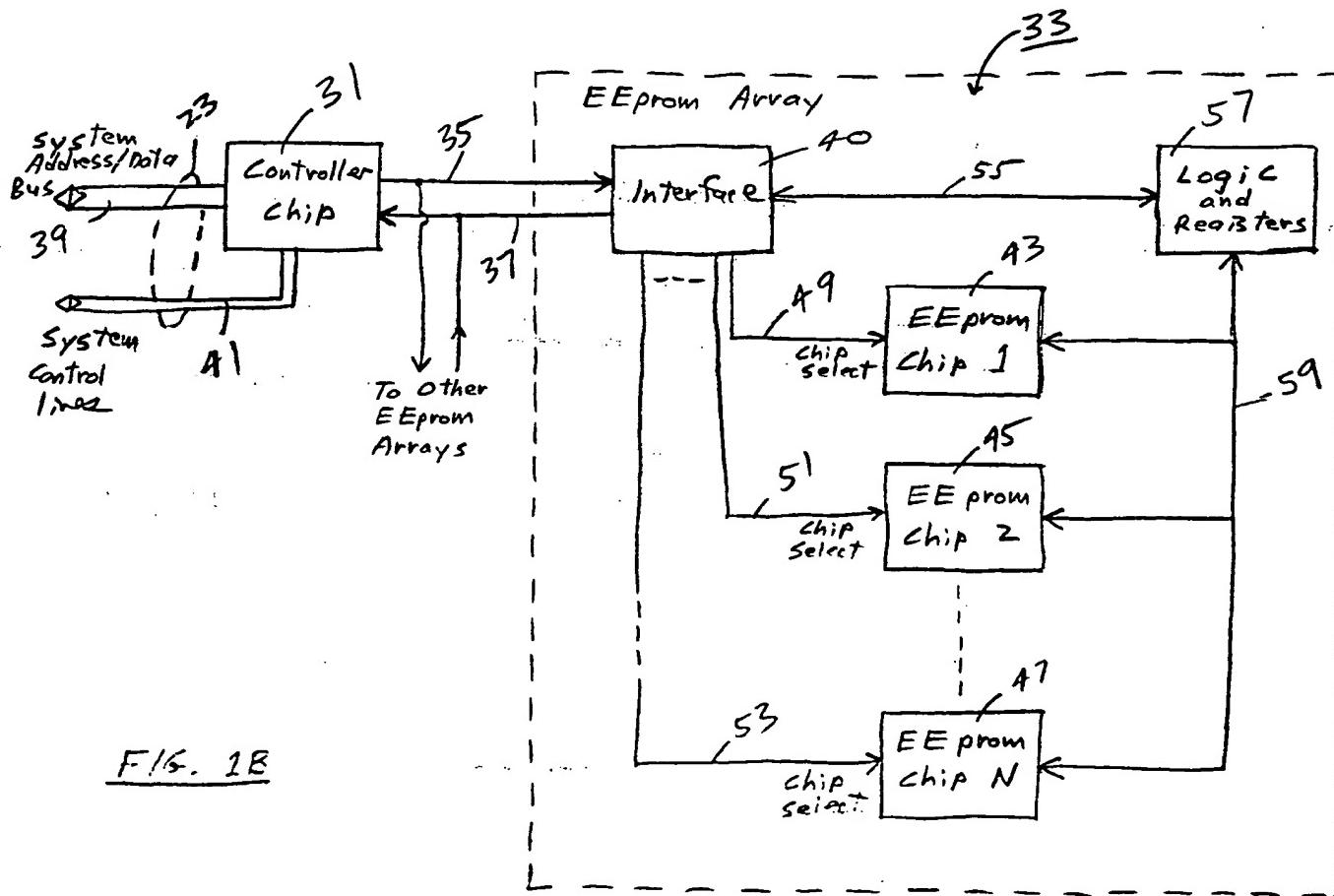
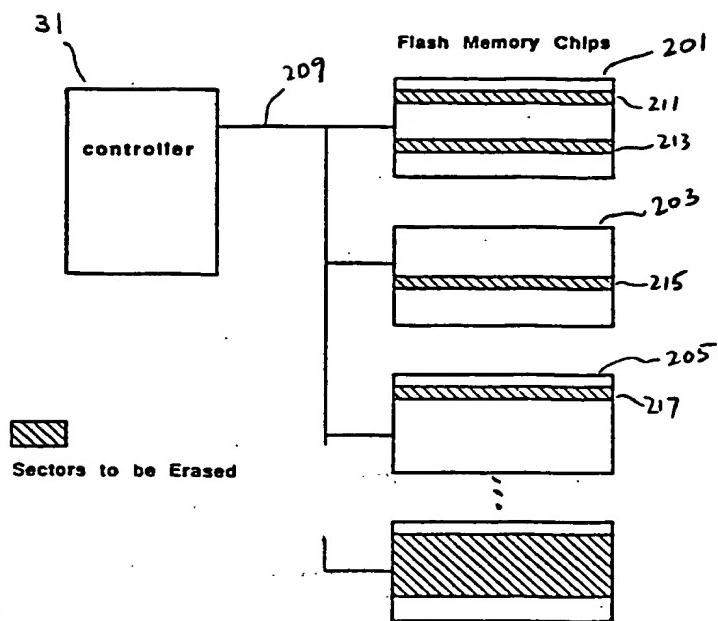


FIG. 1B

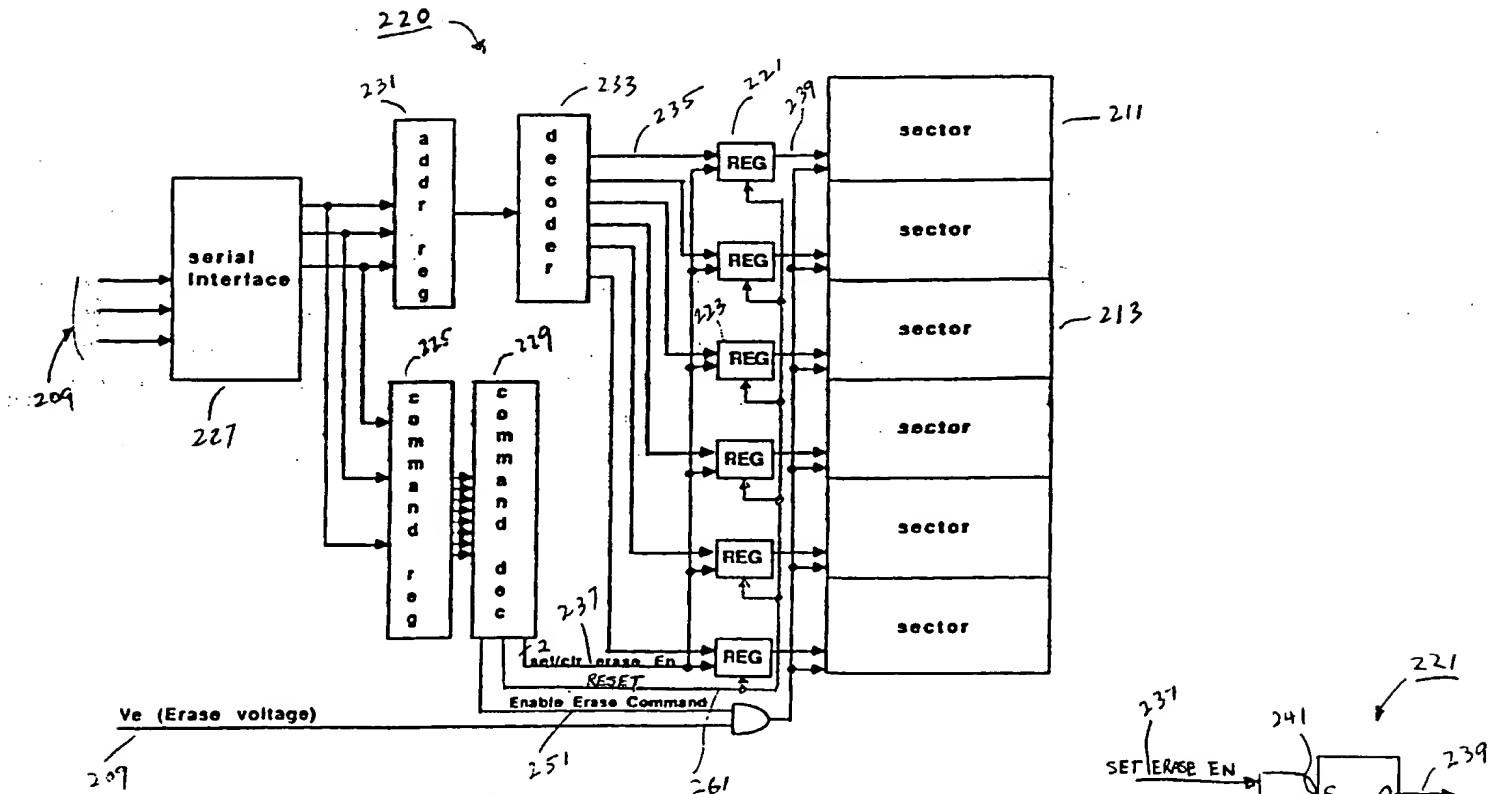
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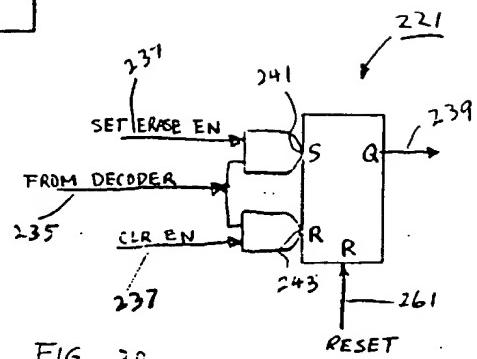
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FIG_2



FIG_3A



FIG_3B

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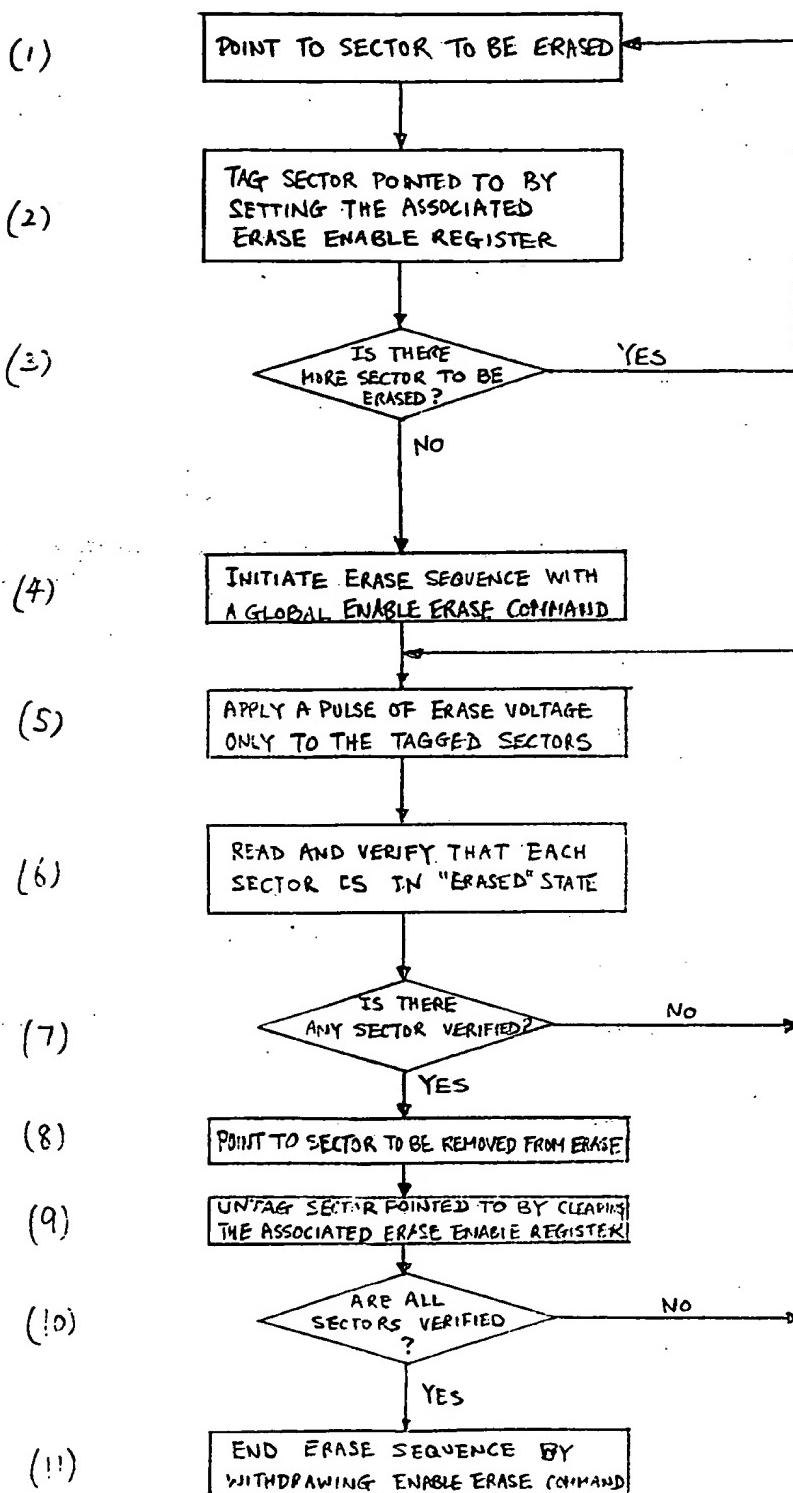
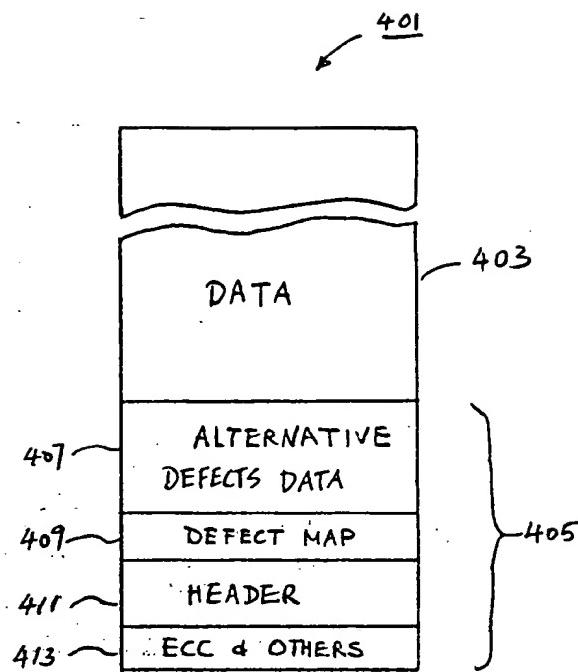


FIG - 4

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SECTOR PARTITION

FIG-5

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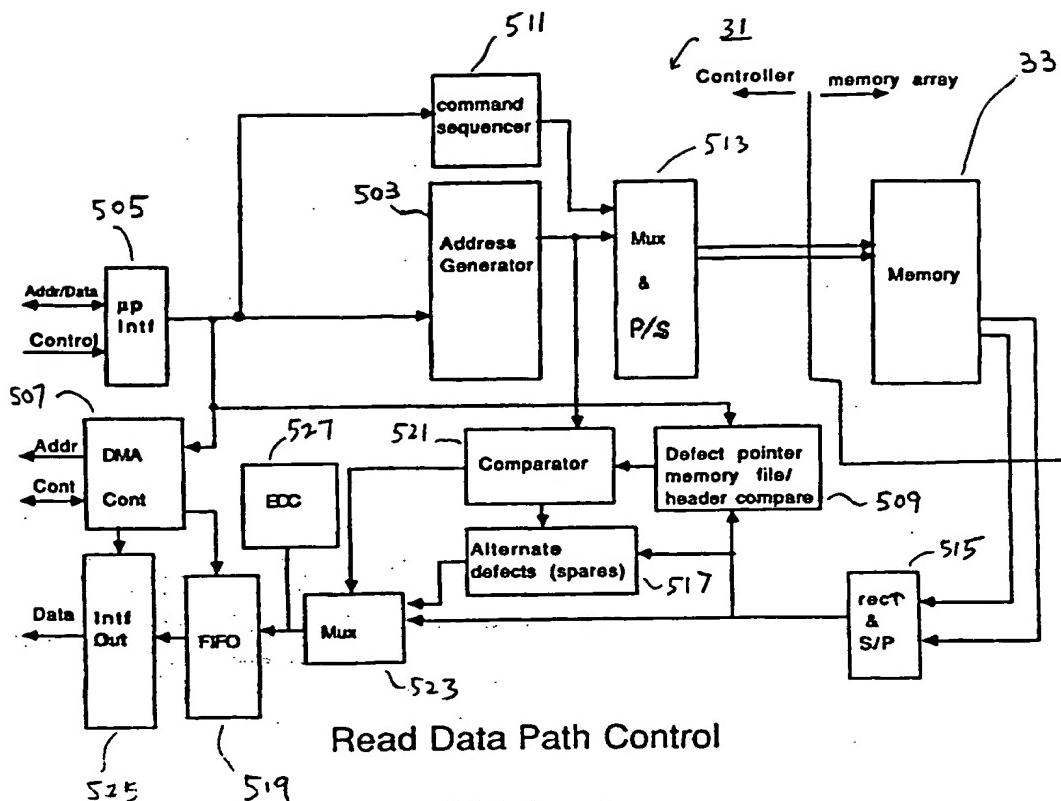


FIG - 6

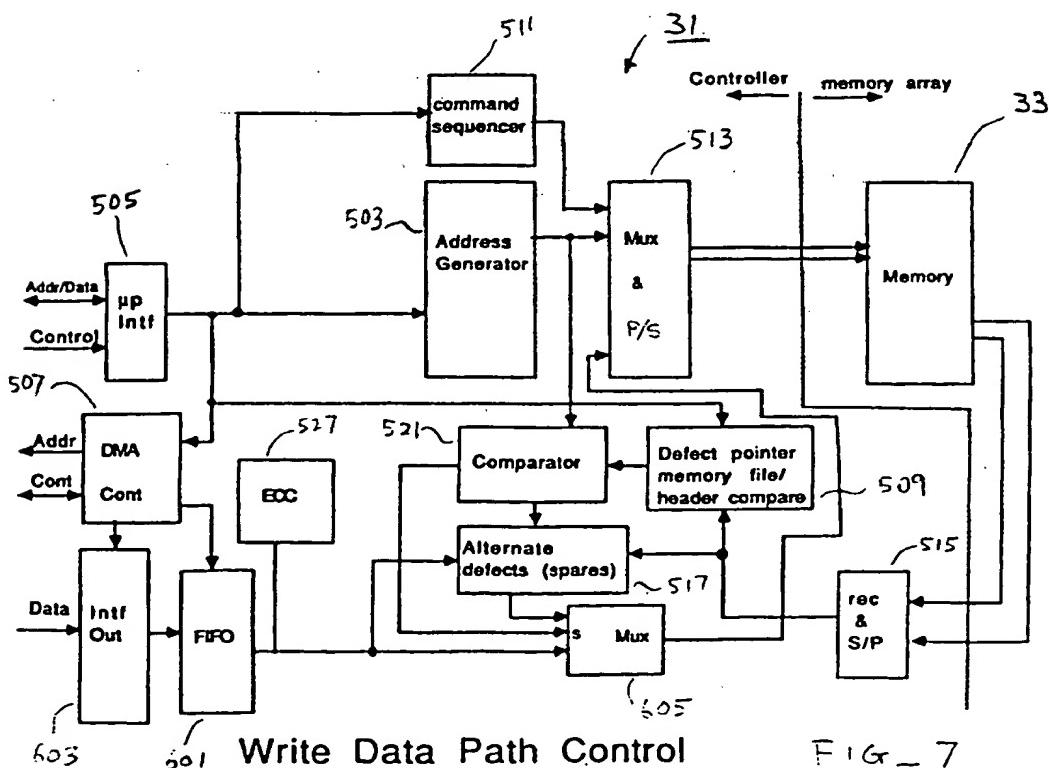


FIG - 7

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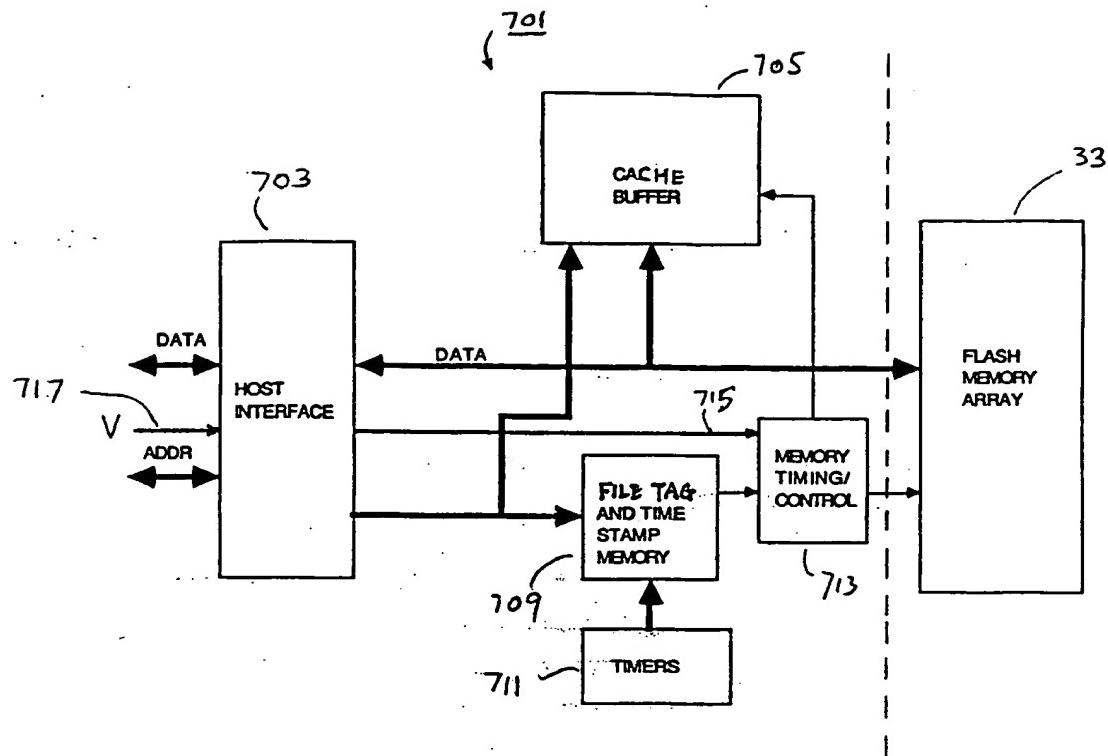


FIG - 8

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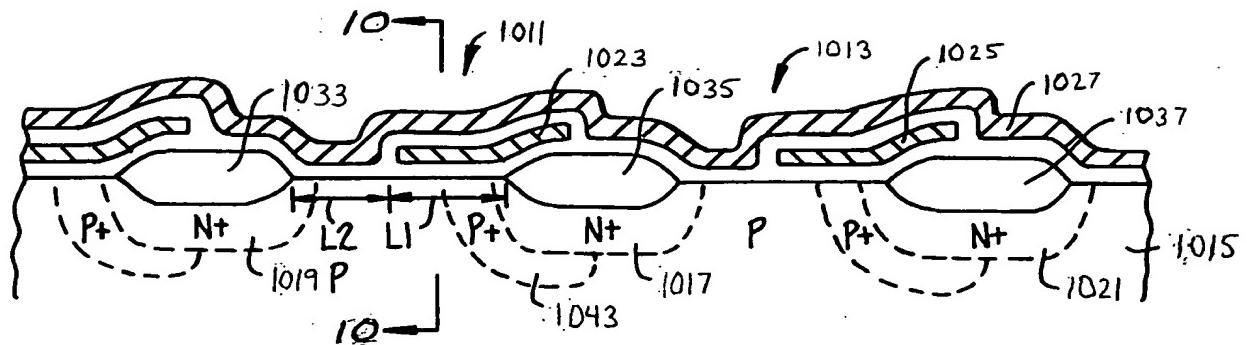


FIG.-E9

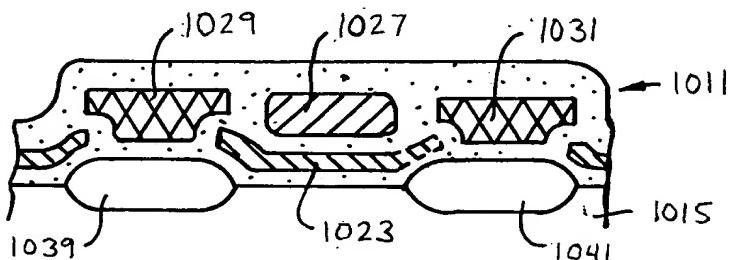


FIG.-E10

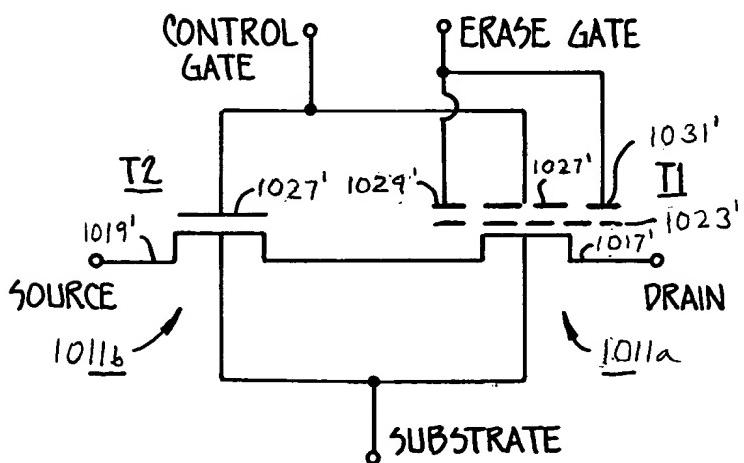


FIG.-E11

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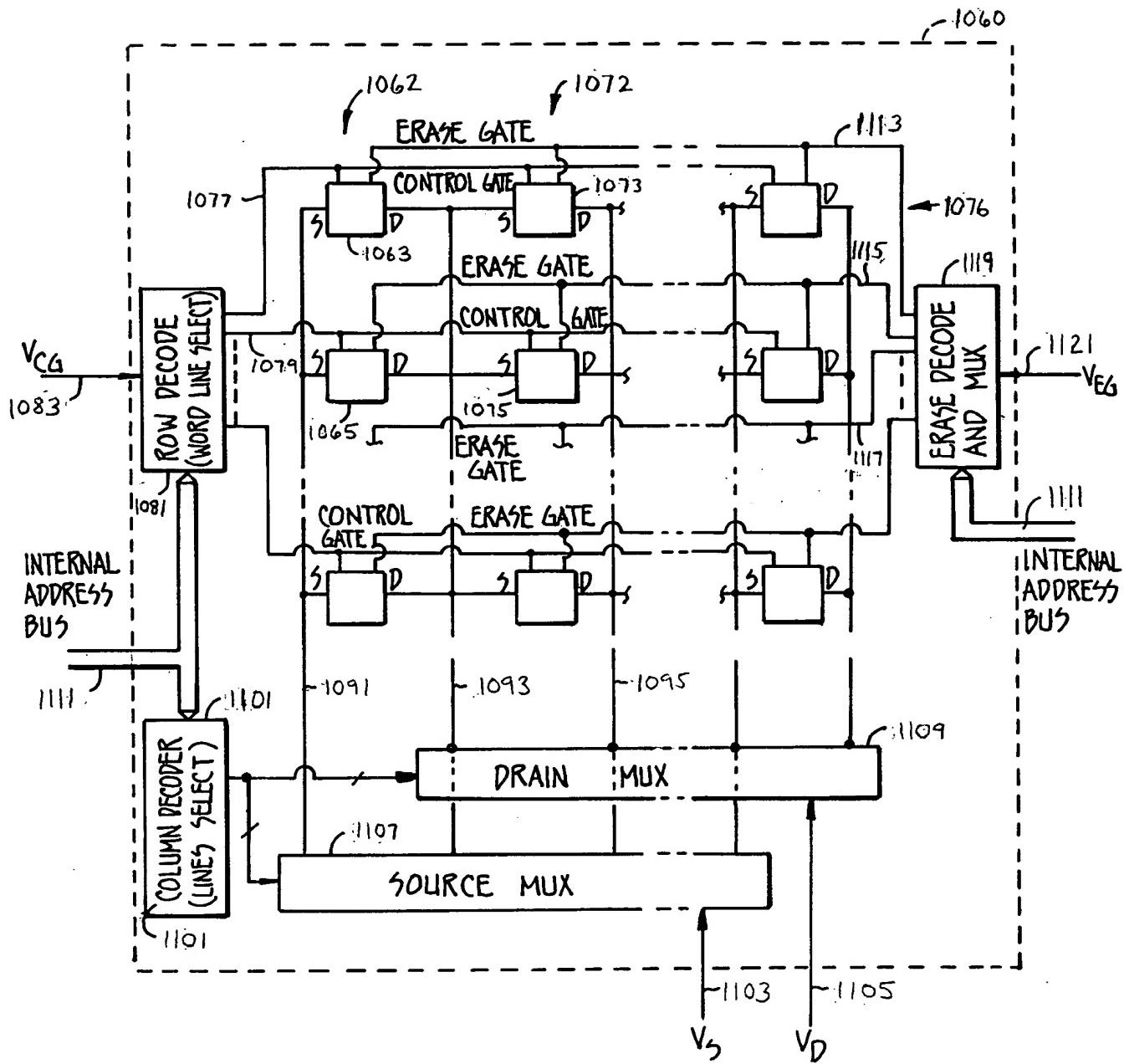
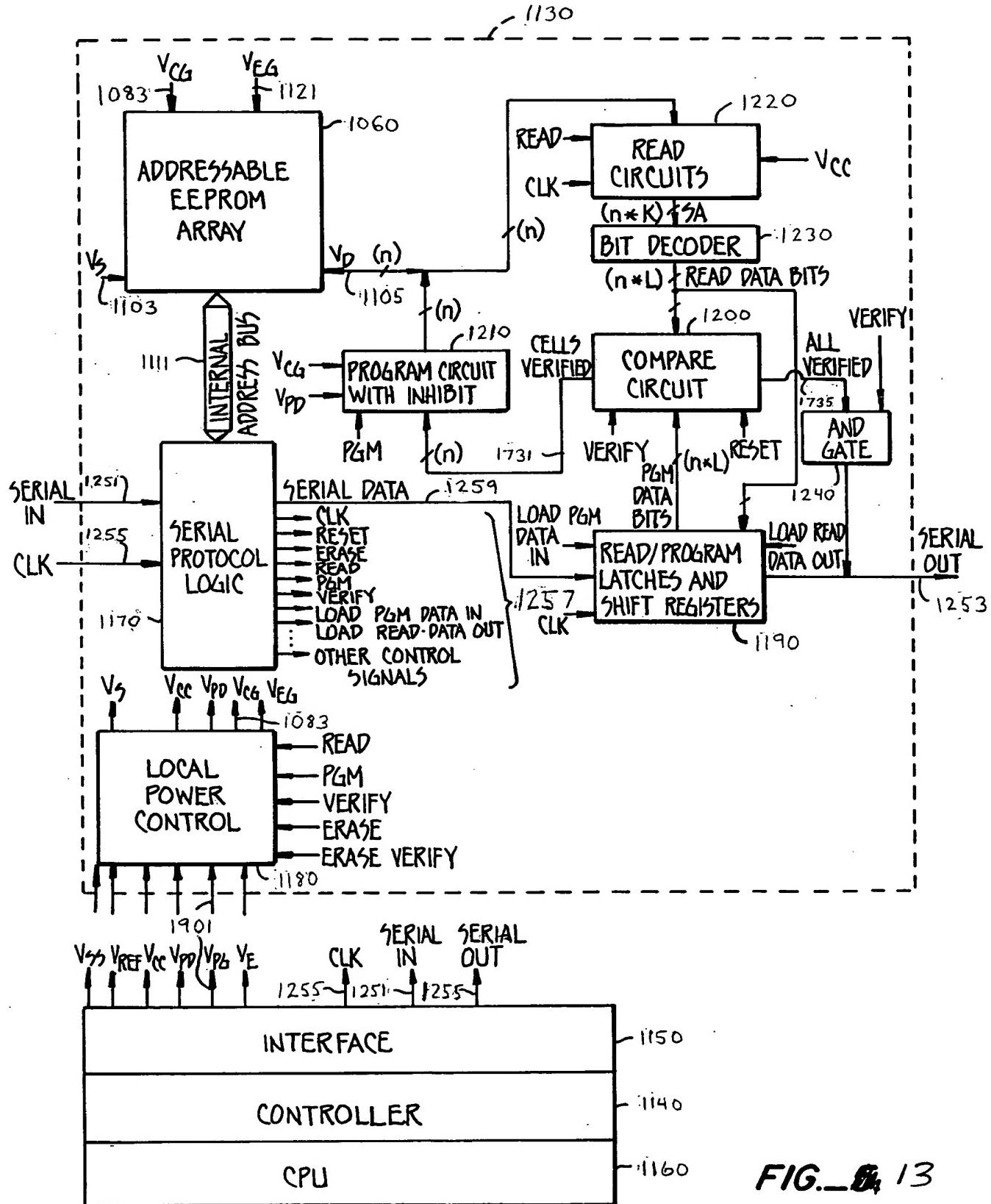


FIG. 12.

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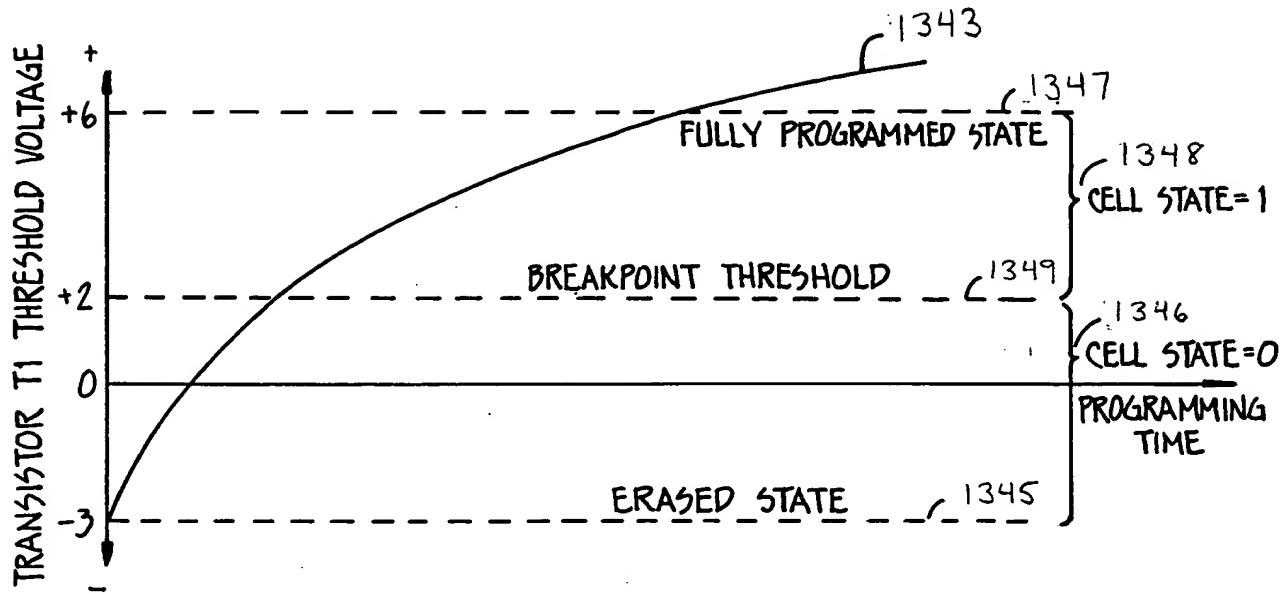


FIG. 14.

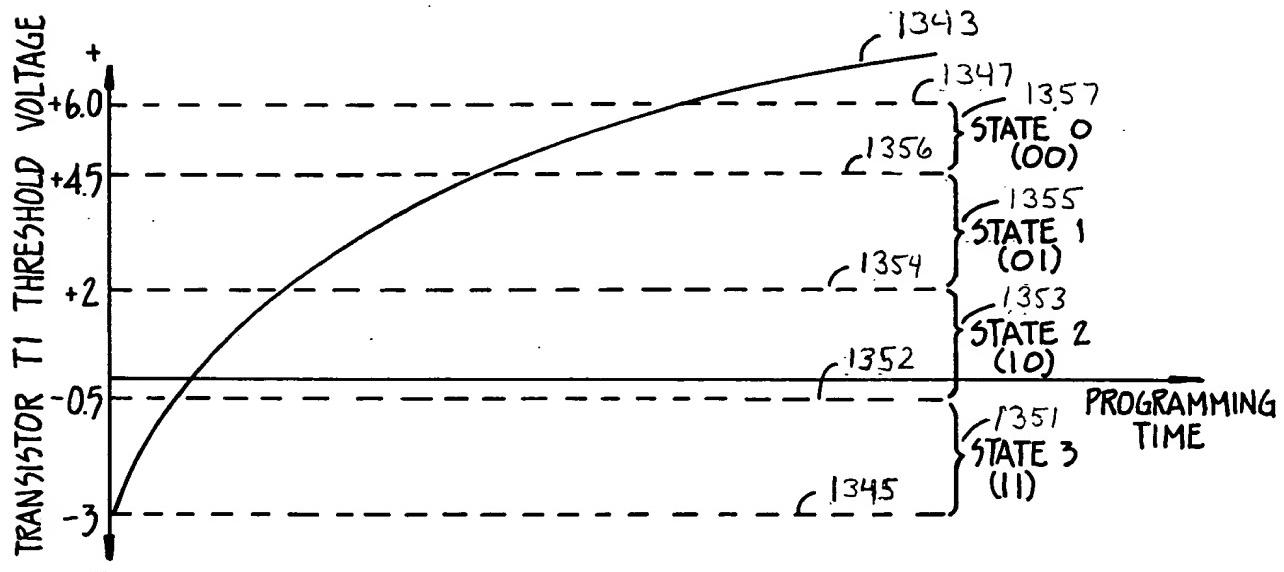


FIG. 14, 15A

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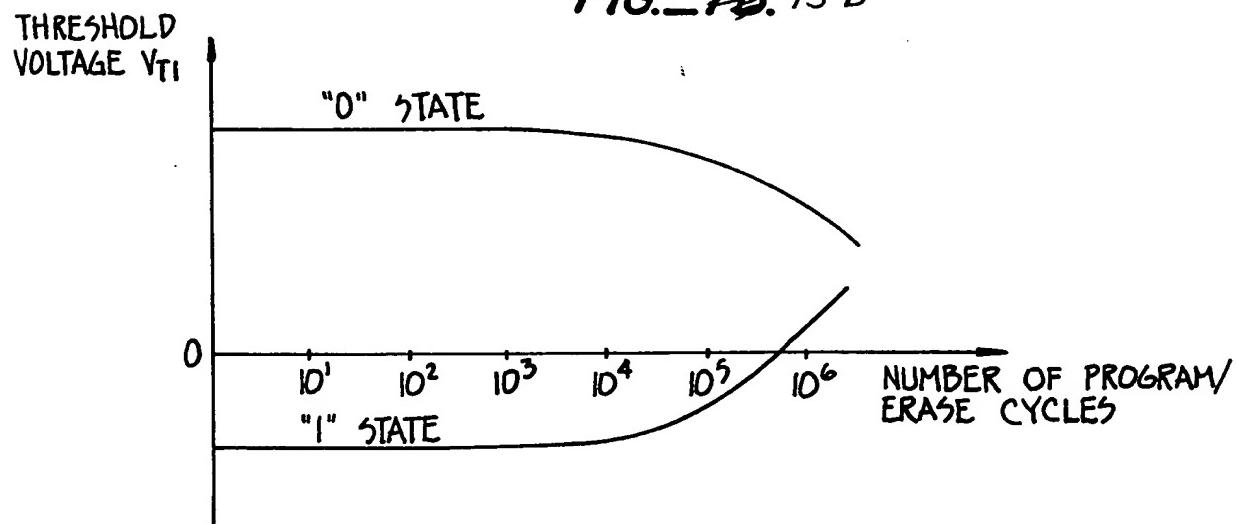
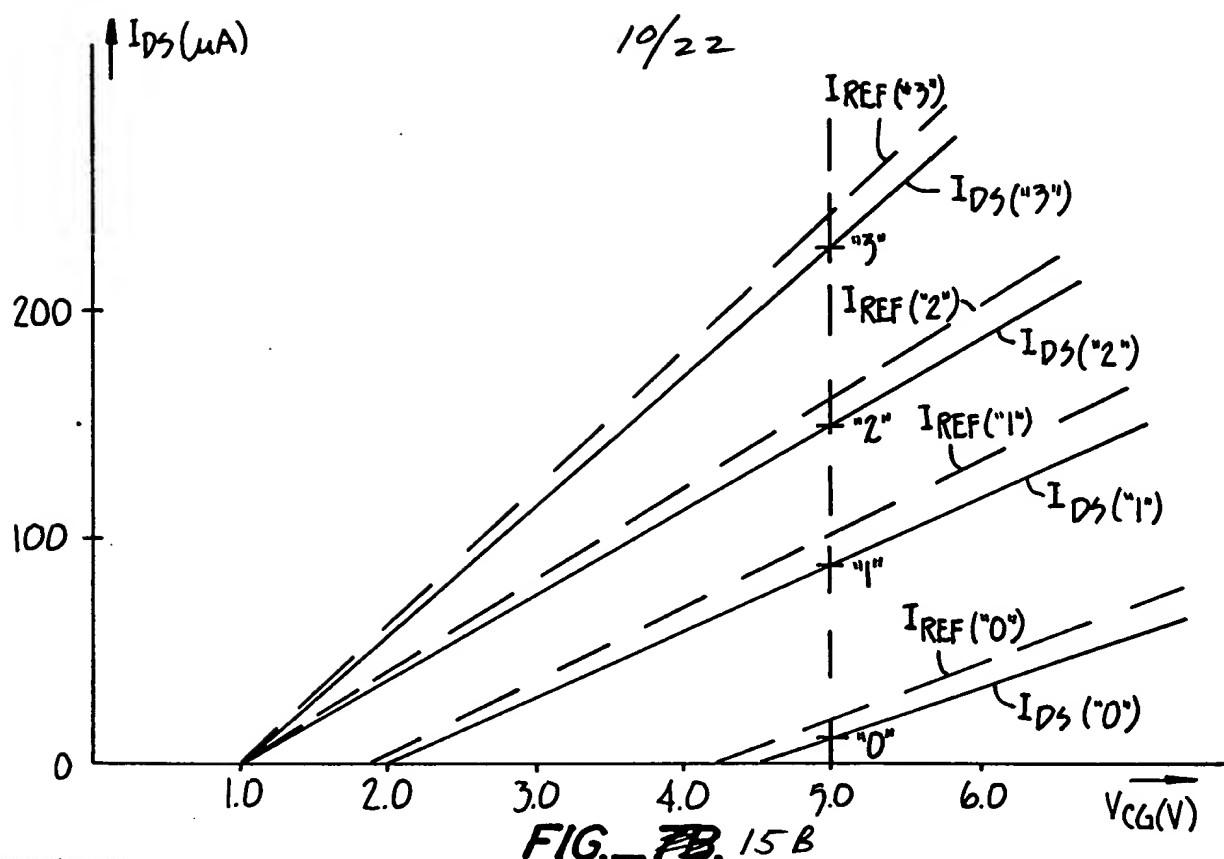
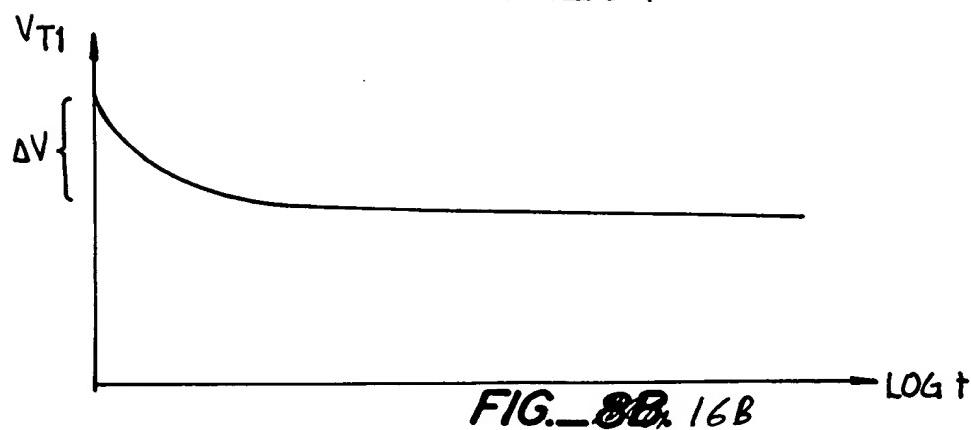


FIG. 16A



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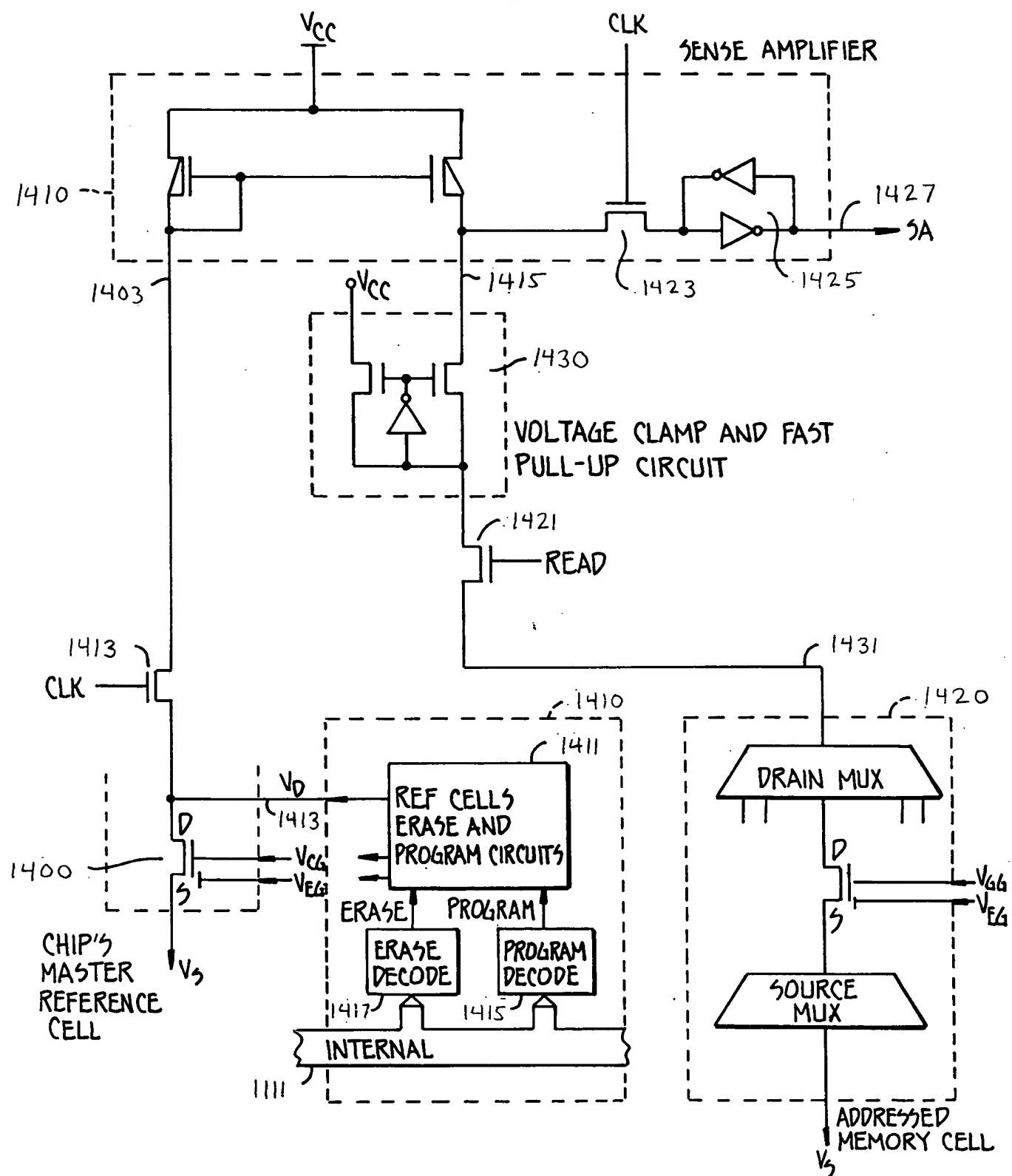


FIG. 17A

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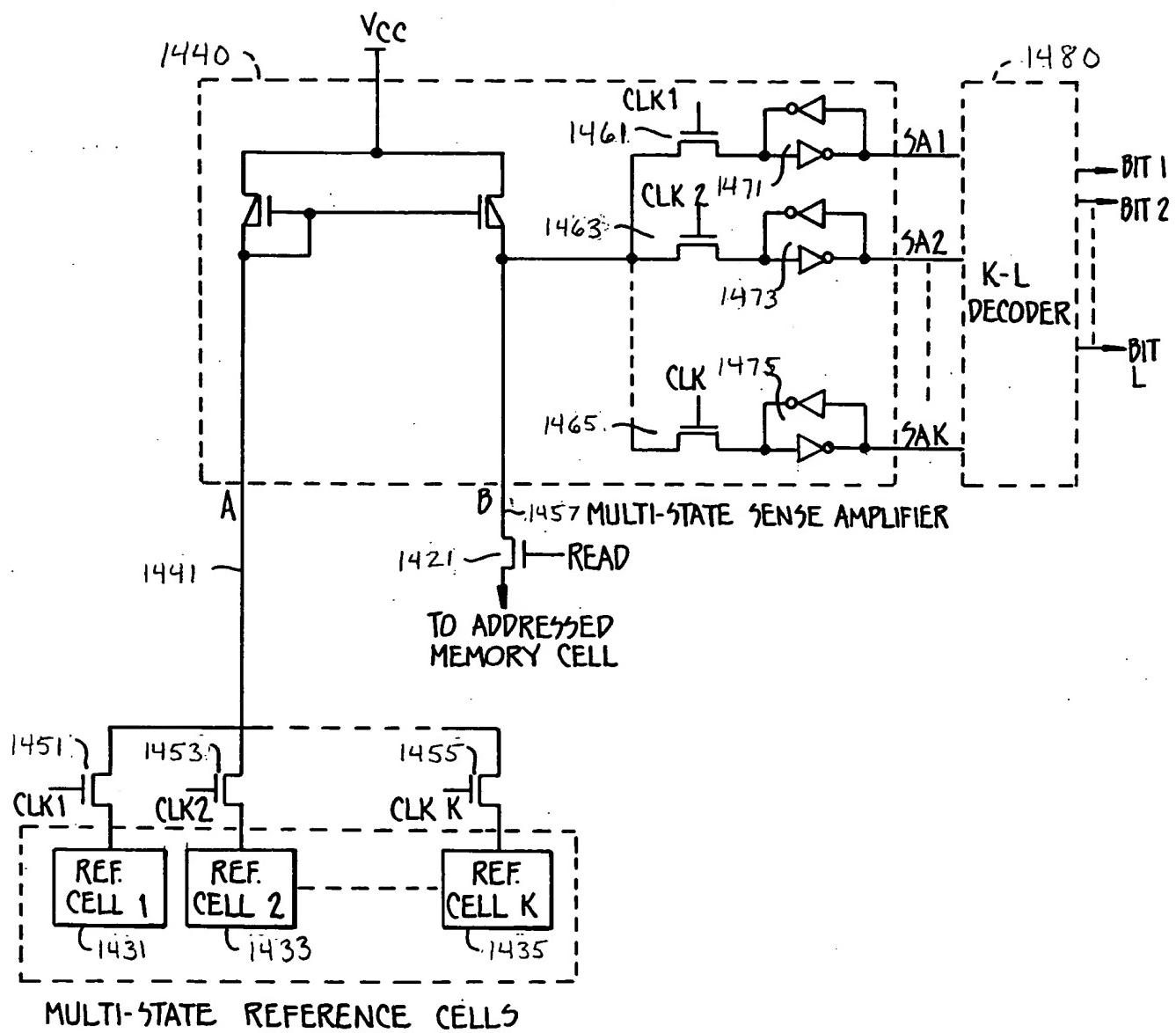


FIG. 2B, 17B

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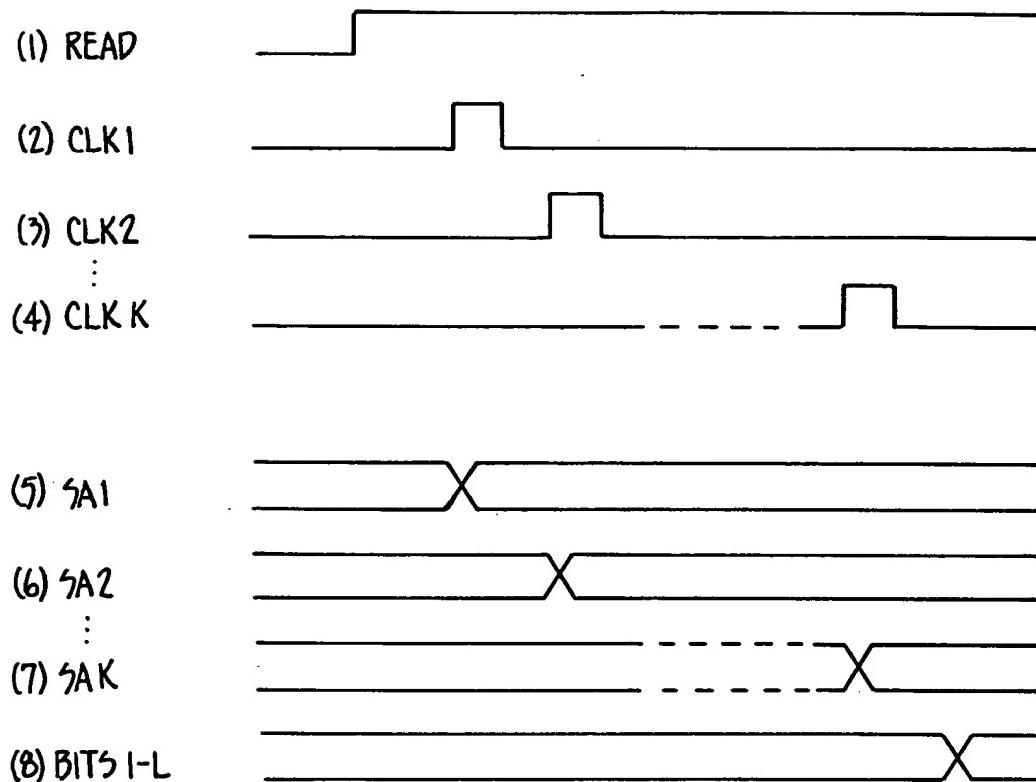


FIG. 17C

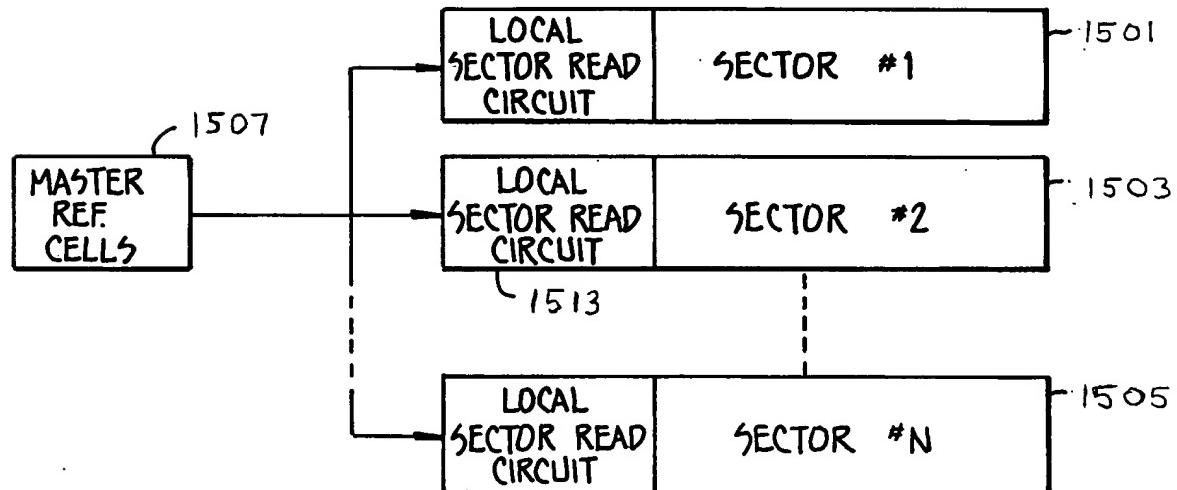


FIG. 18

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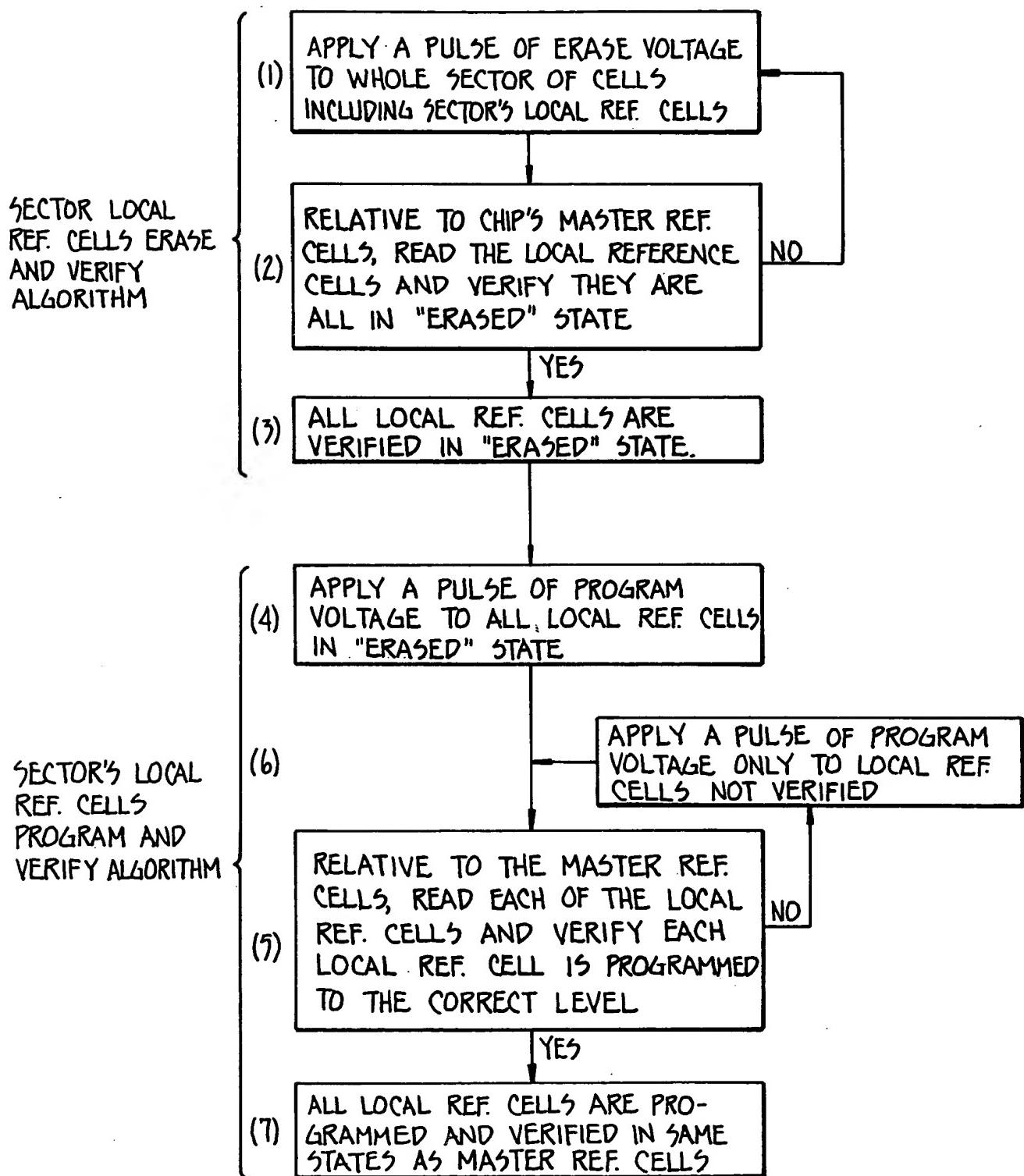


FIG.-# 19

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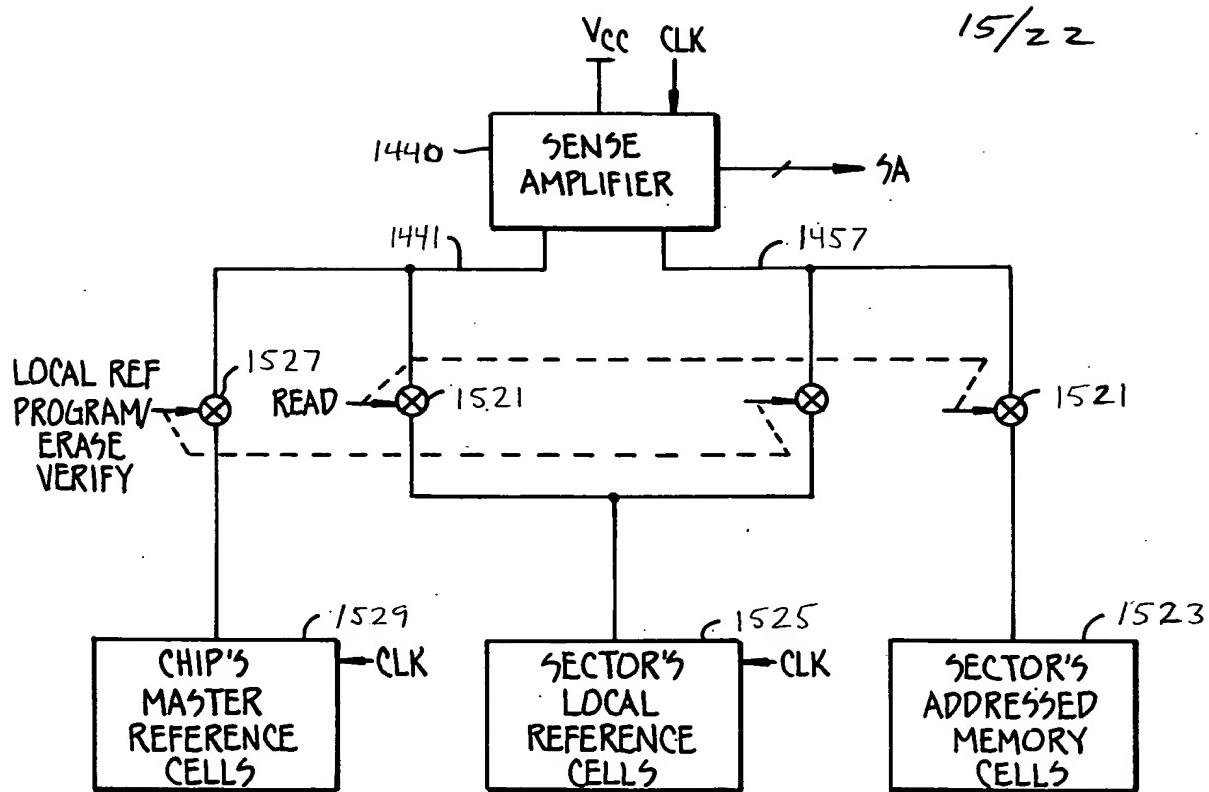


FIG. 12A. 20A

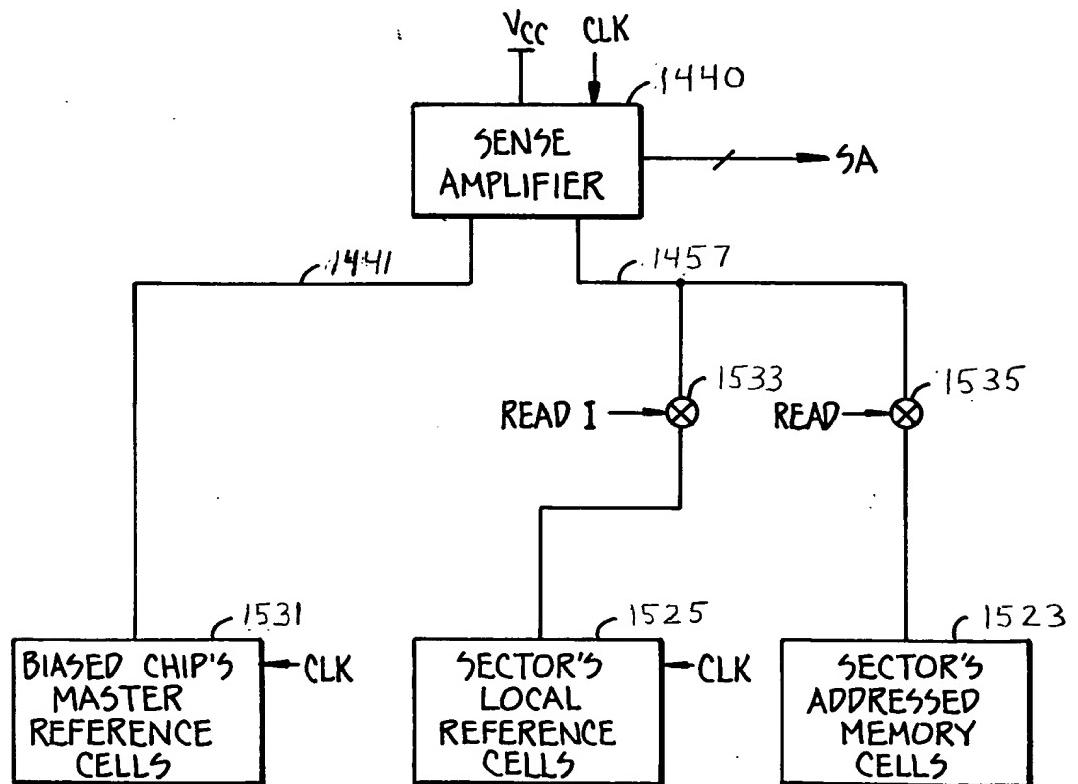


FIG. 13A. 21A

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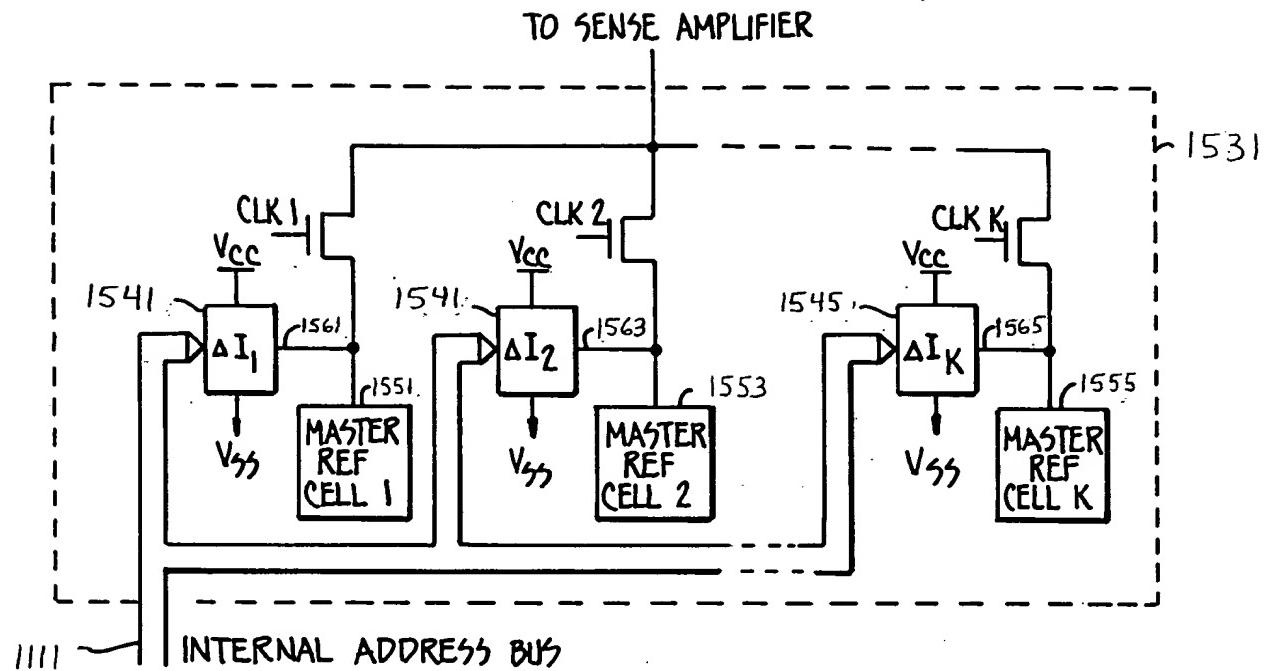


FIG. 21B

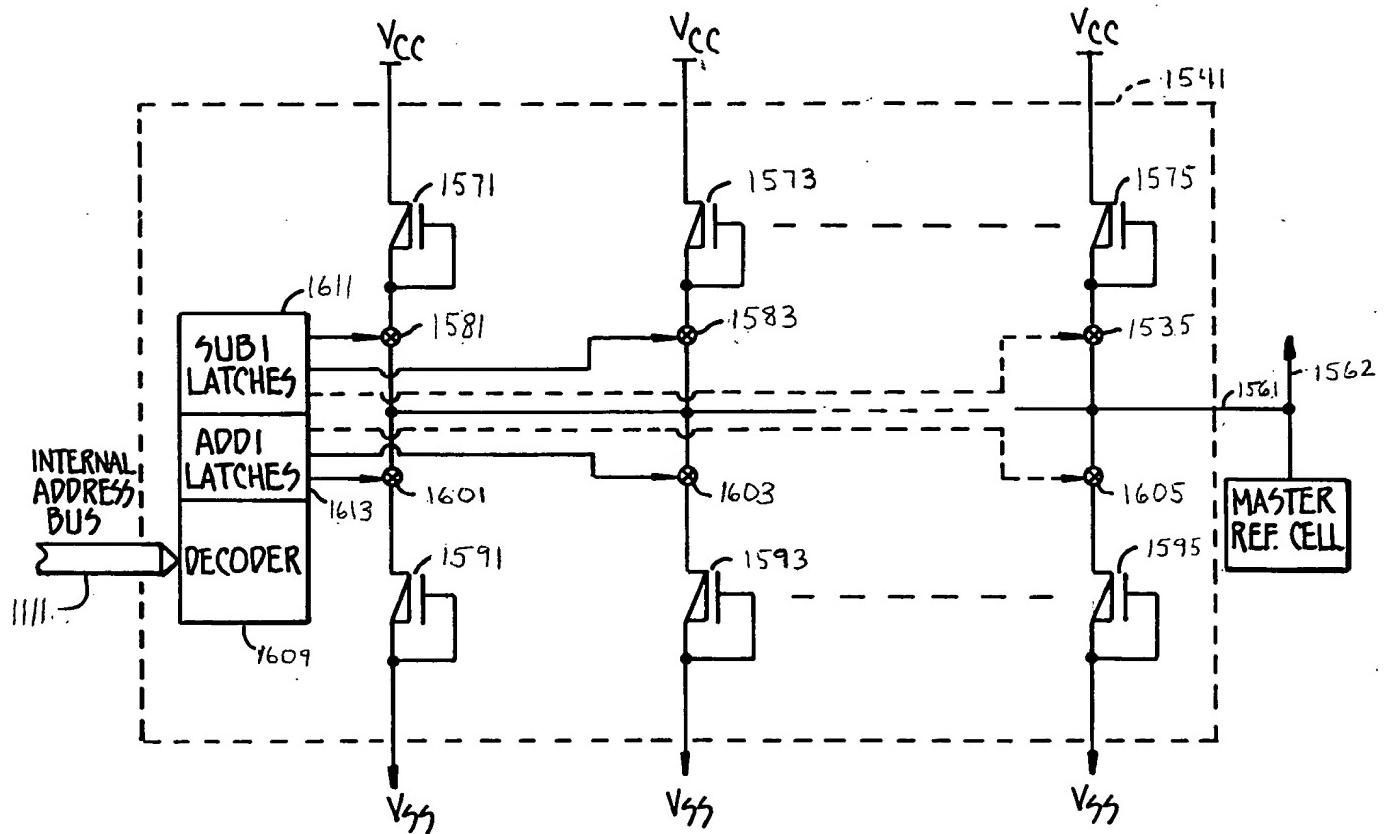


FIG. 21C

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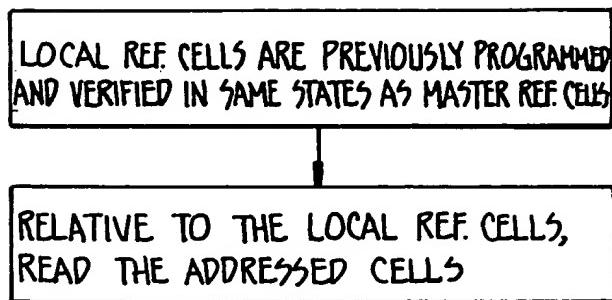


FIG._12B, 20B

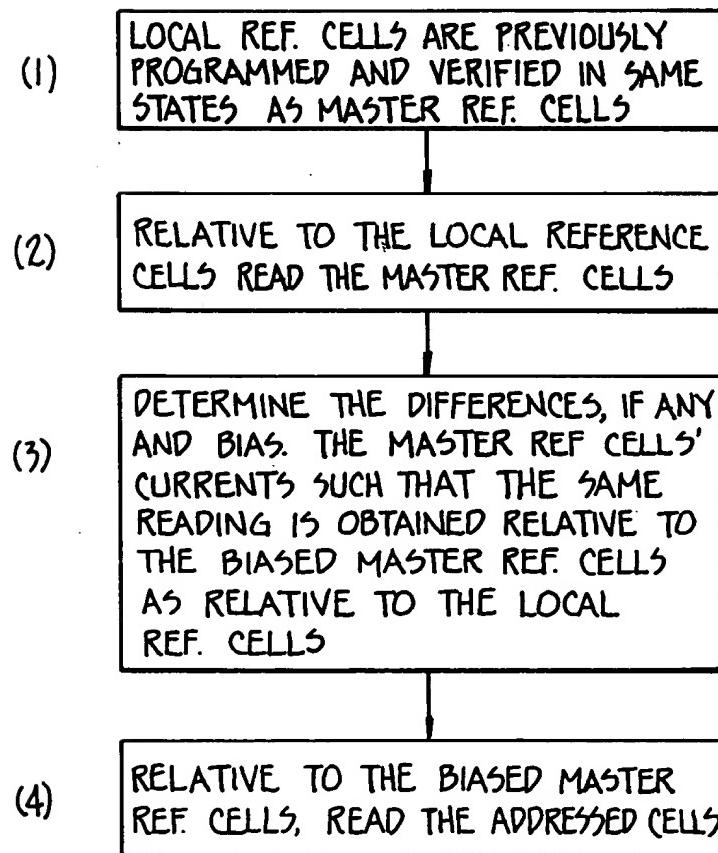
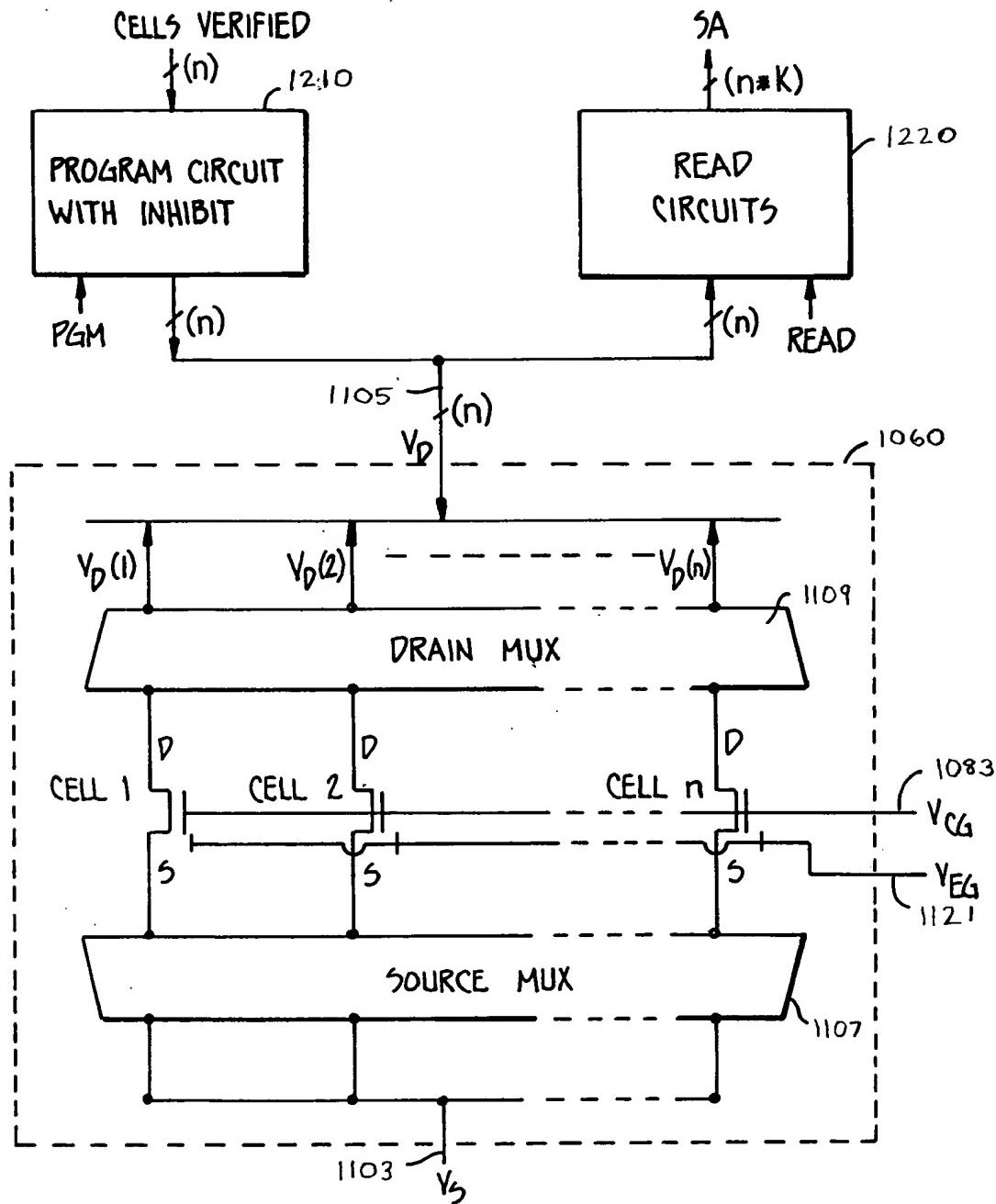


FIG._13D, 21D

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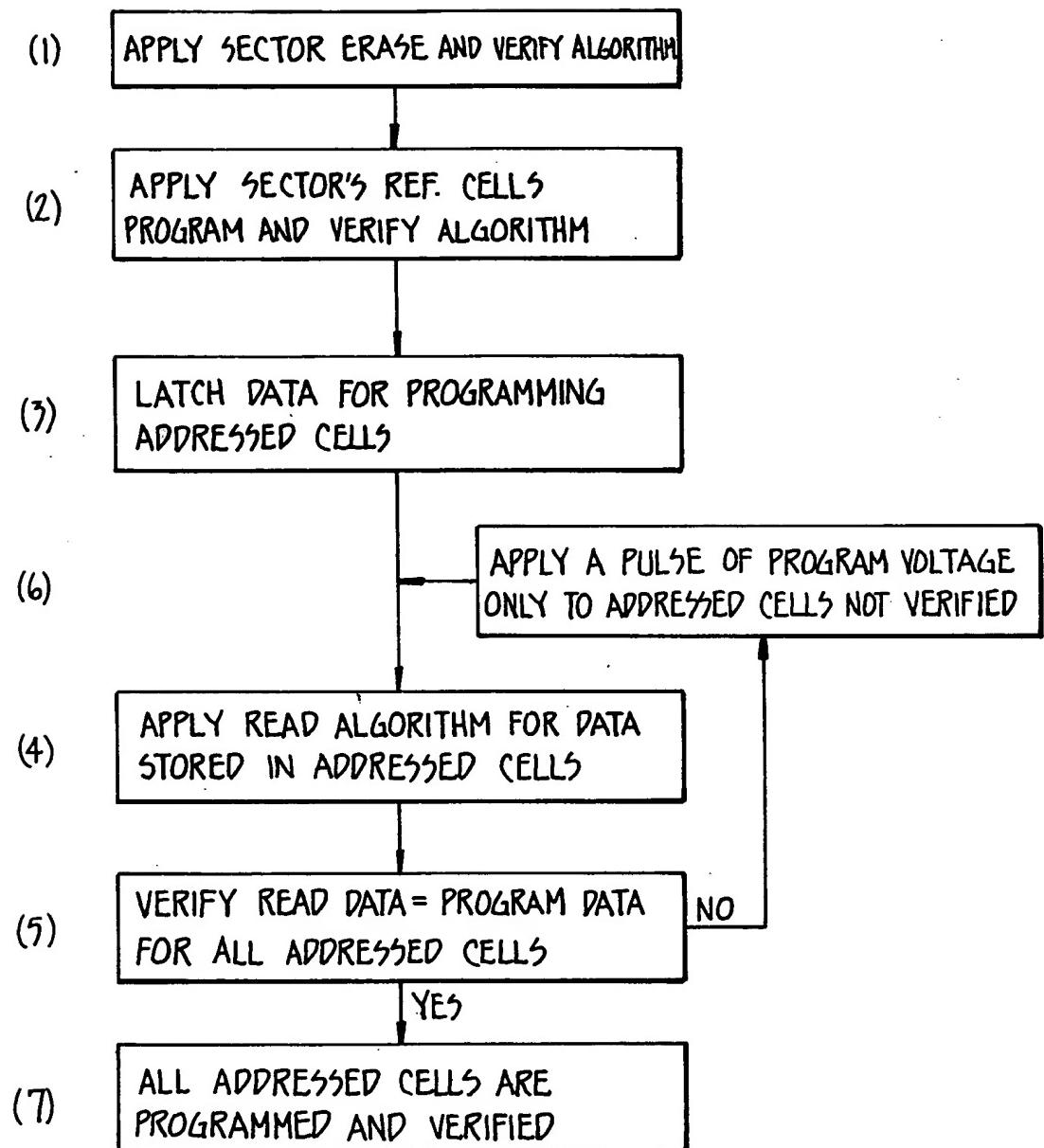


READ/PROGRAM DATA PATHS FOR n CELLS IN PARALLEL

FIG. 22.

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PROGRAM ALGORITHM

FIG. 23

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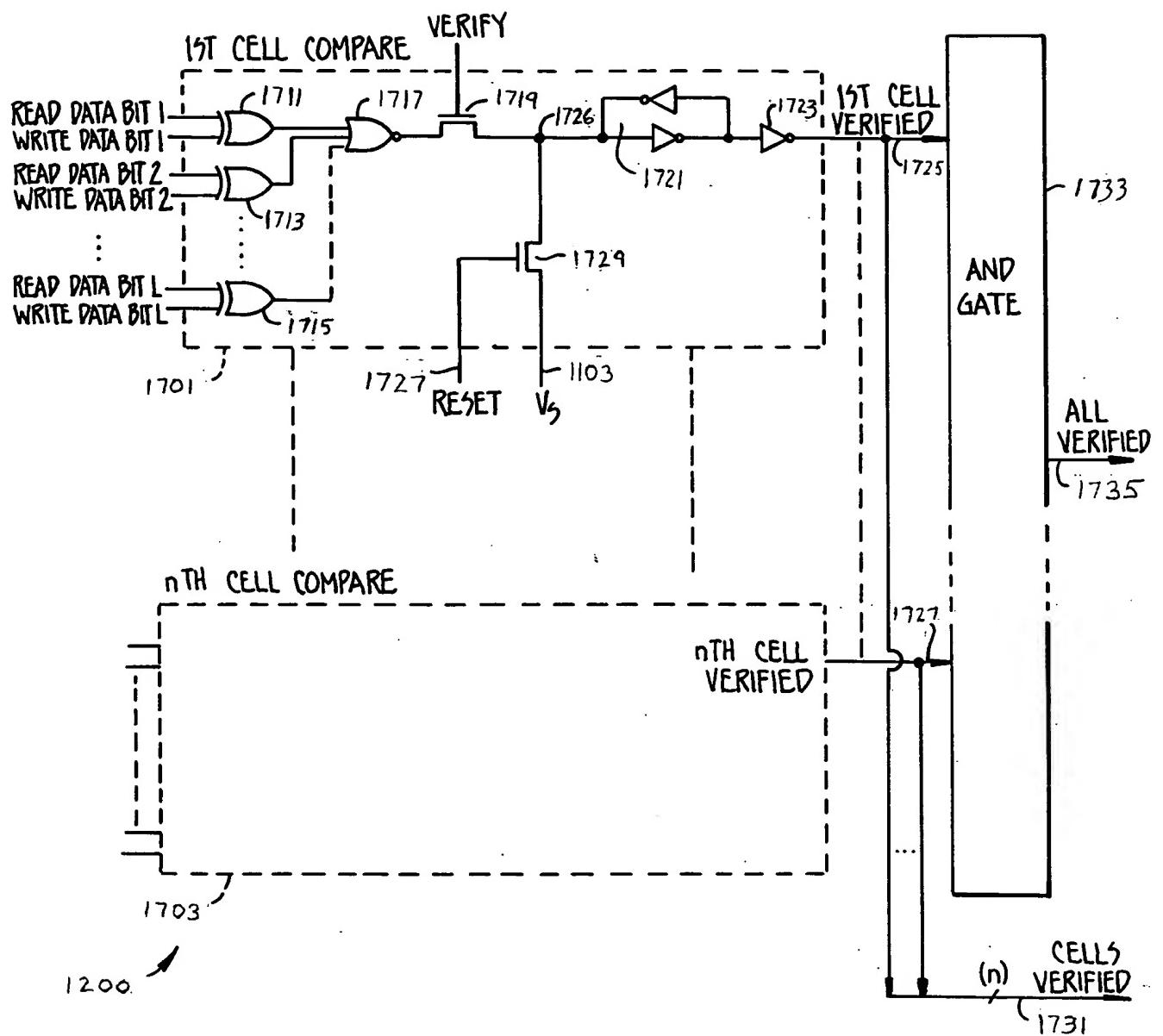


FIG. 24

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z 1/z z

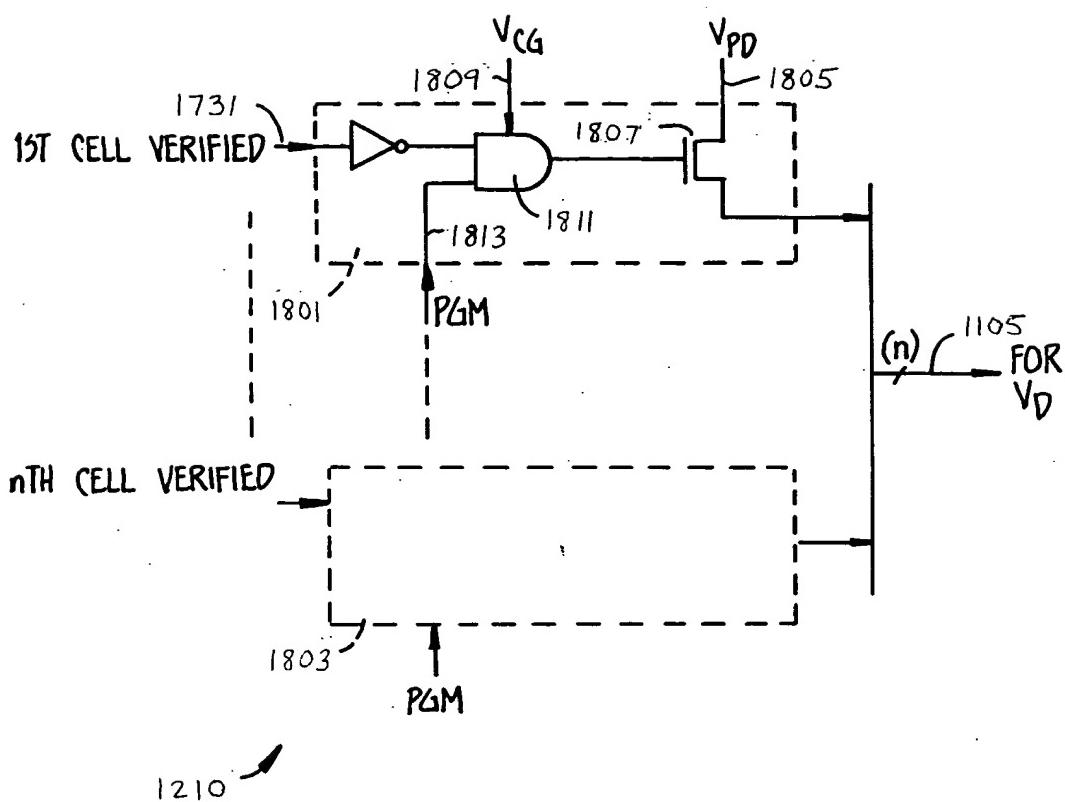


FIG. 25

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	SELECTED CONTROL GATE V_{CG}	DRAIN V_D	SOURCE V_S	ERASE GATE V_{EG}
READ	V_{PG}	V_{REF}	V_{SS}	V_E
PROGRAM	V_{PG}	V_{PD}	V_{SS}	V_E
PROGRAM VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E

~~TABLE 22~~ FIG. 26

(typical values)	READ	PROGRAM	PROGRAM VERIFY	ERASE	ERASE VERIFY
V_{PG}	V_{CC}	12V	$V_{CC} + \delta V$	V_{CC}	$V_{CC} - \delta V$
V_{CC}	5V	5V	5V	5V	5V
V_{PD}	V_{SS}	8V	8V	V_{SS}	V_{SS}
V_E	V_{SS}	V_{SS}	V_{SS}	20V	V_{SS}
unselected control gate	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
unselected bit line	V_{REF}	V_{REF}	V_{REF}	V_{REF}	V_{REF}

$$V_{SS} = 0V, \quad V_{REF} = 1.5V, \quad \delta V = 0.5V - 1V$$

~~TABLE 22~~ FIG. 27